WHITE PAPER

New Paradigm in Application Delivery Networking:

Advanced Core Operating System (ACOS) and Multi-CPU Architecture

The Key to Achieving Availability, Scalability and Performance

By: Lee Chen, CEO of A10 Networks

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Introduction

In today's business environment, companies rely heavily on Web-based applications to communicate and conduct transactions both externally and internally. With more people accessing Websites via smartphones, new third-party applications, news sites, blogs, and social networking/video/picture Websites, Internet traffic to Websites continues to increase significantly and shows no signs of slowing down. More and more processing power is required at data aggregation points, such as load balancers and application delivery controllers.

Answering these demands without incurring escalating costs, many data centers demand that manufacturers of dedicated appliances/servers provide high performance, energy-efficient products in a compact form factor. Many manufacturers intend to ride the latest "Intel Power Curve" to consistently increase the overall performance of their products. Unfortunately, legacy appliance software was designed for single processors. Retrofitting legacy software to new multi-core processor platforms yields results that are less than expected.

The Need for Multi-CPU Architecture

Moore's Law postulates that the number of transistors on a chip doubles every 18 months. But, it has long been known that the shrinking process cannot go on indefinitely. General purpose CPU platforms over the last two decades have gained performance primarily through increasing clock speeds. While this does increase performance, increasing clock speed also increases power consumption and reduces power efficiency on the chip. There has to be another, longer-term solution.

The answer appears to lie in multi-core processors in smaller chips. With increasingly higher speed memory, new multi-core hardware is capable of matching the performance of ASICs. However, high-performance hardware alone will not solve the problem. Today, practical application performance is far behind processor and memory bandwidth advancements. The key issue is in the software. Without a complete redesign of legacy software, the real performance benefits of multi-core appliances can never be realized. The industry needs to have a revolutionary software design to leverage the advancements of multi-core processors. The real solution is to have a scalable, high-performance, highly efficient multi-threaded software architecture tuned for modern, multi-core, multi-processor platforms.

Networking: Silicon Technologies

As noted, customers are looking for high performance, yet flexible, solutions to satisfy their applications' needs. However, the goal of performance is often at odds with the need for flexibility. When designing a network, in order to effectively meet the needs for performance and flexibility, one must understand the differences in the possible silicon technologies. Here is a brief overview.

Application-Specific Integrated Circuits (ASICs) are hard-wired and fixed technology. They are the fastest way to execute specific logic, but there is no room for flexibility. Even a small change to the logic, such as a vulnerability patch, requires fabricating a new chip. This is a costly proposition and can take up to twenty months or more to complete. However, pushing established, static logic into silicon is both cost effective and sensible.

Many companies produce networking ASICs at competitive prices. Other companies offer custom ASIC design and production for niche applications. In some situations, these products are the right solution and can be very effective. This is not true for application delivery networking, however, where the code is complex and requirements are constantly evolving. In these situations, Field Programmable Gate Arrays (FPGAs) may be more appropriate. While not as fast as ASICs, FPGAs offer near-ASIC speeds with the ability to be reprogrammed with new logic as the application needs evolve. The drawback with FPGAs comes during the process of reprogramming. Because programming an FPGA is more similar to designing a chip than developing software, traditional programming techniques cannot be used, complicating and lengthening the development process. FPGAs can be an effective high performance solution when a system is architected properly.

Another specialized type of processor is the Network Processor (NP). NPs are programmable chips that promise to make switches, routers and other network devices faster and more efficient. On paper, NPs appear to be a good solution, but they have never lived up to expectations. There are several issues. Since each NP vendor uses a different, proprietary design, programming microcode is difficult and not portable. In addition, NP cache sizes are often smaller with higher costs than general purpose Intel/AMD, PowerPC and MIPS cache sizes, creating unpredictable, slower data plane processing. While NPs can offload a limited amount of application traffic, they lack the flexibility and expandability to handle Layer 7 application traffic.

AX Series with Advanced Core OS (ACOS) for Multi-CPU Architecture

Since A10's beginning in late 2004, the company has focused its engineering resources on developing the revolutionary Advanced Core OS (ACOS). ACOS was engineered to provide Application Delivery Networking with scalability, flexibility and manageability. ACOS is designed specifically for a Symmetric Multi-Processing (SMP), shared memory architecture. ACOS runs on A10's AX Series platform and provides high performance, intelligence and low latency for high volume Internet applications.

ACOS eliminates the inefficiency associated with traditional multi-processing architectures. The traditional approaches for multiprocessing may incur significant overhead – inter-process communication (IPC) among different processors/threads, inefficient memory locks for simultaneous data access, and overhead in thread scheduling and switching. The ACOS architecture has no IPC overhead, no context switching, and highly efficient simultaneous shared memory access.

With the revolutionary Advanced Core Operating System (ACOS), the AX Series delivers a family of Advanced Traffic Managers and provides the best price/performance per watt for the Internet Application Delivery market. Its hardware uses modern, high performance multi-core processors, Flexible Traffic ASICs (FPGA), Layer 2/3 switch ASICs, and Acceleration SSL ASICs in an energy-efficient, compact form factor.

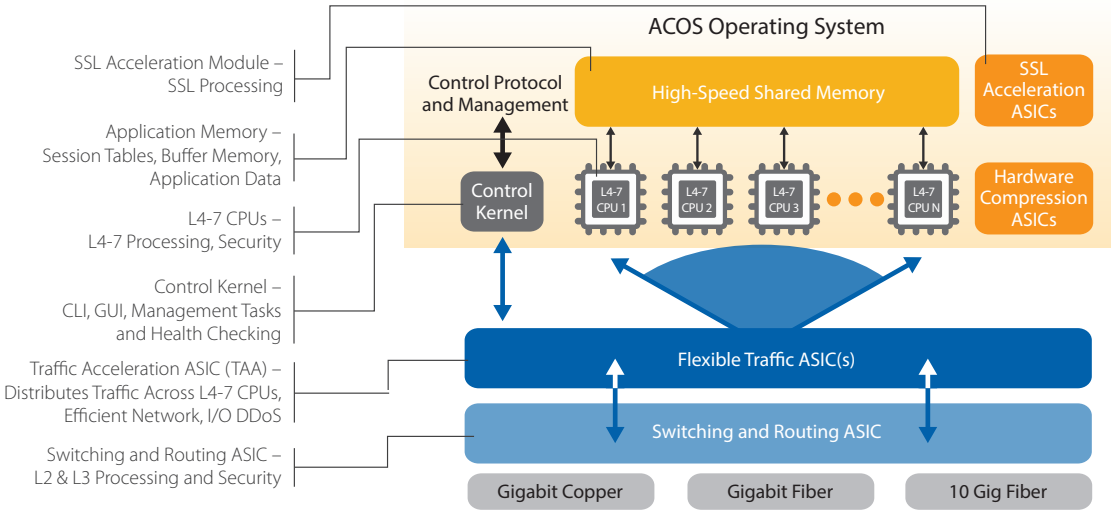
The ACOS architecture enables the AX Series to deliver industry-leading performance by adopting modern merchandised hardware chipsets. In addition, ACOS is portable and not dependent on any particular CPU architecture. Because ACOS virtualizes the processing resource away from the actual logic, a change in CPU platform does not require substantial changes to ACOS itself. By design, ACOS can take advantage of constant advancements in processing platforms and is ready for the future.

Advanced Core Operating System (ACOS) Architecture

The AX Series was developed by A10's award-winning Silicon Valley-based engineers. This group of experienced specialists in high performance Layer 2/3 switching, Layer 4-7 applications and super-computing system design created ACOS from the ground up to optimize performance, taking clear advantage of the features and benefits of a multi-CPU, multi-core system.

A10's ACOS is the secret sauce that provides these key features:

- Hardware-based dynamic flow distribution to multiple cores (CPUs)
- Hardware-based buffer management
- Hardware-based transmit assist
- Wire-speed security features such as SYN flood protection
- Integrated Layer 2-3 switching with Layer 4-7 application delivery



The recent introduction of Parallel Flexible Traffic ASIC technology further increases application throughput and DDoS SYN flood protection.

ACOS also includes the following key technologies:

- A control kernel independent of the packet data threads
- Dynamic and robust Layer 4-7 application traffic distribution among all data CPUs
- The optimized Layer 4-7 packet data threads run on all data CPU(s)
- Layer 4-7 application data processing with near-zero locking and near-zero memory contention
- Traffic processing offloads for data threads; specifically, control plane, Layer 2/3 traffic, traffic distribution, buffer management, SSL encryption/decryption and SYN-defense are offloaded to ASICs
- Optimized non-blocking TCP/IP stack
- Optimized non-blocking SSL driver
- Zero-copy buffer management is the key to high performance Layer 7 applications
- Layer 4-7 protocol optimizations
- Layer 4-7 high-availability
- IPv4 and IPv6 protocol optimizations

ACOS provides the industry's leading multi-processing architecture to solve Application Delivery problems such as slow application response times and poor application performance. ACOS, in combination with AX's multi-CPU hardware, is designed to fully utilize all the processing cores and ride the performance curves of modern hardware architectures. ACOS enables the AX Series to provide high performance and flexibility, which is needed to meet the evolving demands of the Internet Application Delivery market as new applications are introduced.

About A10 Networks

A10 Networks is a leader in application networking, providing a range of high-performance application networking solutions that help organizations ensure that their data center applications and networks remain highly available, accelerated and secure. Founded in 2004, A10 Networks is based in San Jose, California, and serves customers globally with offices worldwide. For more information, visit: **www.a10networks.com**

Corporate Headquarters

A10 Networks, Inc
3 West Plumeria Ave.
San Jose, CA 95134 USA
Tel: +1 408 325-8668
Fax: +1 408 325-8666
www.a10networks.com

Worldwide Offices

North America
sales@a10networks.com
Europe
emea_sales@a10networks.com
South America
brazil@a10networks.com
Japan
jinfo@a10networks.com
China
china_sales@a10networks.com
Taiwan
taiwan@a10networks.com
Korea
korea@a10networks.com
Hong Kong
HongKong@a10networks.com
South Asia
SouthAsia@a10networks.com
Australia/New Zealand
anz_sales@a10networks.com

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